Evaluation of Field-Effect Mobility and Contact Resistance of Transistors That Use Solution-Processed Single-Walled Carbon Nanotubes

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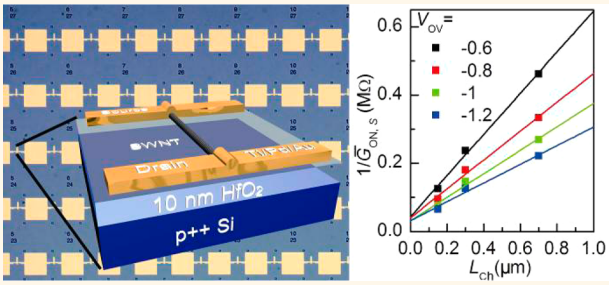
ABSTRACT



Solution-processed single-walled carbon nanotubes (SWNTs) offer many unique processing advantages over nanotubes grown by the chemical vapor deposition (CVD) method, including capabilities of separating the nanotubes by electronic type and depositing them onto various substrates in the form of ultradensely aligned arrays at low temperature. However, long-channel transistors that use solution-processed SWNTs generally demonstrate inferior device performance, which poses concerns over the feasibility of using these nanotubes in high-performance logic applications. This paper presents the first systematic study of contact resistance, intrinsic field-effect mobility (μ_{FE}), and conductivity (σ_m) of solution-processed SWNTs based on both the transmission line method and the Y function method. The results indicate that, compared to CVD nanotubes, although solution-processed SWNTs have much lower μ_{FE} for semiconducting nanotubes and lower σ_m for metallic nanotubes due to the presence of a higher level of structural defects, such defects do not affect the quality of electric contacts between the nanotube and metal source/drain electrodes. Therefore, solution-processed SWNTs are expected to offer performance comparable to that of CVD nanotubes in ultimately scaled field-effect transistors, where contacts will dominate electron transport instead of electron scattering in the channel region. These results show promise for using solution-processed SWNTs for high-performance nanoelectronic devices.

KEYWORDS: carbon nanotube · transistor · solution processed · electron transport · contact resistance

Single-walled carbon nanotubes (SWNTs) are a promising material to complement or even replace Si in future high-performance and/or low-power logic circuits and radio frequency devices.[1−3] Ballistic field-effect transistors (FETs) based on SWNTs have been scaled down to sub-10 nm channel length (L_{Ch}) and deliver excellent performance owing to their ultrathin body and nearly transparent electrical contact.[4,5] Meanwhile, SWNT FETs with long L_{Ch} demonstrate exceptional diffusive transport properties with field-effect mobility (μ_{FE}) up to 10 000 $cm^2\ V^{-1}\ s^{-1}$.[6,7] These devices, however, are all based on SWNTs grown by the chemical vapor deposition (CVD) method, especially the highly linear and long aligned nanotubes grown on single-crystalline quartz substrates.[5,7−9] Although CVD growth produces SWNTs with a high level of structural perfection, and therefore the best electrical performance, those as-synthesized nanotubes are a mixture of metallic (*m*-SWNTs) and semiconducting nanotubes (*s*-SWNTs). An effective method for removing *m*-SWNTs after CVD growth without affecting neighboring *s*-SWNTs over a large scale has not yet been established. In addition to the challenge of *s*-SWNT purity, to be considered for a practical technology, the nanotube density must be increased to a certain level to provide sufficient current output per unit device width. As-synthesized, CVD-grown nanotube arrays typically have tube densities in the range of 1−10 tubes/μm. Multiple growth[10,11] or transfer printing[12,13] schemes, whose scalability over entire wafers and manufacturability are unclear, can increase the nanotube density up to ~50 tubes/μm. However, in order to outperform Si devices, nanotube density above 200 tubes/μm must be realized.[14]

Rather than working to increase the purity and density in CVD-grown arrays of SWNTs, another approach is to first suspend nanotubes (synthesized by one of several bulk methods) in solution, perform separation and assembly, and then deposit them onto substrates for device fabrication. In recent years, great progress has been made

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in separating SWNTs according to their electronic type in solution by techniques including density gradient ultracentrifugation,[15,16] selective polymer wrapping,[17,18] and chromatography.[19,20] A separated nanotube solution with *s*-SWNT purity above 99% can be readily obtained in the laboratory and is commercially available. In addition, ultradensely packed aligned SWNT arrays with tube densities as high as 100−500 tubes/μm can be prepared from solution *via* methods such as DNA scaffold-assisted assembly[21] and Langmuir−Blodgett technique (unpublished experiment), making solution-processed nanotubes very attractive for the above-mentioned applications. Although solution-suspended SWNTs offer several processing advantages, transistors that use such nanotubes generally show inferior performance, with reported average effective mobility for *s*-SWNTs ($\bar{\mu}_{eff}$) in the range of 20−200 $cm^2\ V^{-1}\ s^{-1}$,[22−24] as compared to CVD tubes, whose $\bar{\mu}_{eff}$ is typically above 1000 $cm^2\ V^{-1}\ s^{-1}$.[6−8] This discrepancy could originate from either high contact resistance, which is especially detrimental to electron transport for the relatively short solution-processed nanotubes, or strong scattering in the channel region from structural defects of nanotubes,[25−27] likely induced by high-power sonication and/or strong-acid treatments during purification and suspension processes.

To assess the feasibility of using solution-processed nanotubes in ultrascaled quasi-ballistic FETs, it is important to understand the determining factor that leads to the lower performance of conventional diffusive transistors that use solution-processed nanotubes. In the present paper, we first obtain the L_{Ch} dependence of averaged device parameters from a collection of FETs that use solution-processed *s*-SWNTs in the submicrometer regime and extract averaged intrinsic μ_{FE} ($\bar{\mu}_{FE}$) and average contact resistance ($\bar{R}_{C,S}$) by the transmission line method (TLM).[28] We then acquire these same metrics of each device/nanotube based on the Y function method (YFM),[29] which helps to verify the results obtained *via* TLM and allows us to analyze device-to-device variability. The scaling properties of solution-processed *m*-SWNTs are also examined. The results indicate that for solution-processed nanotubes, although extracted μ_{FE} of *s*-SWNTs and conductivity of *m*-SWNTs are inferior to those of CVD tubes, their contact resistances are comparable. Therefore, it is feasible to develop high-performance nanoelectronic technologies based on solution-processed SWNTs because they will offer performance comparable to that of CVD tubes in ultimately scaled nanotube FETs, where the nanotube−metal contact properties exert much more influences on device operation than diffusive transport properties inside the channel.

RESULTS AND DISCUSSION

Figure 1a depicts a schematic illustration of a FET based on a solution-processed SWNT, which uses

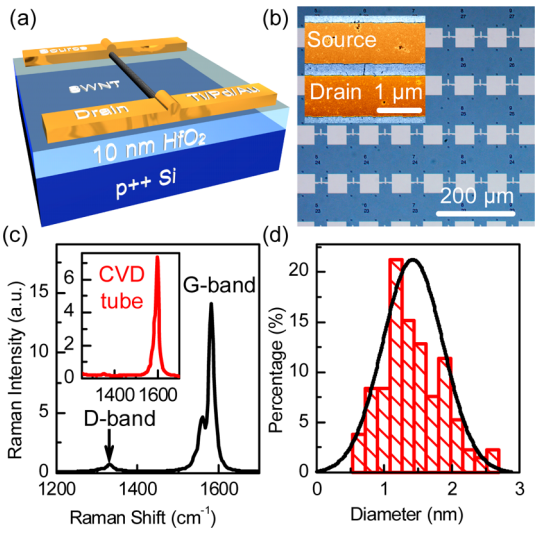

Figure 1. (a) Schematic illustration of a single nanotube FET fabricated on 10 nm HfO_2/p++ Si substrate with Ti/Pd/Au as S/D contact. (b) Optical image of an array of such devices fabricated on the same wafer. Pattern of probe pads was designed to be compatible with a semi-automatic probe station capable of measuring hundreds of such devices with high throughput. Inset: False-colored SEM image of a typical device. (c) Raman spectrum of solution-processed SWNTs at 532 nm excitation, showing characteristic D-band and G-band of nanotubes. Inset: Raman spectrum of CVD-grown aligned SWNTs on quartz substrate. (d) Diameter distribution of over 130 SWNTs produced by arc-discharge method and suspended in 1,2-dichloroethane (DCE) as measured by AFM. The black solid line is Gaussian fit to the data.

heavily doped p-type (p++) Si as its gate electrode and 10 nm HfO_2 deposited by CVD as the gate dielectric. Source/drain (S/D) electrodes were defined by electron-beam lithography (EBL) and lift-off of Ti (0.2 nm)/Pd(15 nm)/Au(20 nm). Hundreds of such devices with L_{Ch} of 150, 300, and 700 nm were fabricated on the same wafer, as shown in Figure 1b, and about 20% of the devices contain a single nanotube channel. The inset of Figure 1b is a false-colored scanning electron microscopy (SEM) image of a typical device. The quality of the as-deposited SWNTs was determined by Raman spectroscopy. Figure 1c shows a Raman spectrum sampled from a spot covering a number of nanotubes deposited on a substrate, near their characteristic tangential G-band peak located at ~1580 cm^{-1}. A very small defect-induced disorder D-band peak appears at ~1330 cm^{-1}.[30] The G-band/D-band peak ratio is above 20, which is typical for high-purity and high-quality solution-processed nanotubes[31] but somewhat lower than that of pristine CVD-grown SWNTs synthesized on ST-cut single-crystalline quartz substrates according to previously reported procedures,[8] whose G-band/D-band peak ratio measured with the same setup is about 45, as shown in the inset, indicating the presence of a higher level of structural defects in solution-processed SWNTs. Figure 1d provides the diameter distribution of deposited SWNTs measured by atomic force microscopy

(AFM) in tapping mode. The nanotube diameter is critical for associated device performance since it heavily influences band gap and μ_{FE} of the nanotube as well as the height of the Schottky barrier formed at the nanotube−metal contacts.[6,32,33] The average diameter of our solution-processed nanotubes is ~1.4 nm, which is comparable to that of CVD-grown nanotubes.[7,8]

Figure 2a shows output characteristics of a typical single-tube FET based on a solution-processed *s*-SWNT with 150 nm L_{Ch}, and Figure 2b plots a collection of transfer curves for devices with ON/OFF ratios of drain current (I_{DS}) greater than 1000. Note that these FETs show a wide variation of threshold voltage (V_T) caused by both the distribution of nanotube diameter and residual charges or traps in the channel.[34] To minimize the influence of V_T variation, we extrapolate the apparent threshold voltage (V_{Text}) of each device from the linear segment of the transfer curve, and we use gate overdrive voltage (V_{OV}), defined as gate voltage (V_{GS}) in excess of V_{Text}, for data analysis. It is worth noting that V_{Text} is smaller than intrinsic V_T with the presence of non-negligible contact resistance.[29] The distribution of *s*-SWNT FET drain-to-source conductance in the ON state ($G_{ON,S}$) under V_{OV} of −1.2 V is illustrated in Figure 2c. As-fabricated SWNT FETs demonstrate a range of $G_{ON,S}$, partially due to the existence of nanotube diameter variation. Statistical averaging was performed to reduce the impact of this variation, which allows for the use of standard TLM to extract $\bar{\mu}_{FE}$ and $\bar{R}_{C,S}$. These average numbers are used to benchmark with averaged properties of CVD tubes extracted from nanotube arrays and provide a first-order projection of such parameters for a hypothetical device based on an array of parallel solution-processed *s*-SWNTs as the device channel.

Figure 2d presents the resistance ($1/G_{ON,S}$) of each device measured under V_{OV} of −1 V as a function of L_{Ch}, with the averaged resistance for each L_{Ch} and the corresponding standard deviation highlighted in red. The dependence of the resistance of a *s*-SWNT on L_{Ch} can be modeled as $R_{total} = 2R_{C,S} + R_{Ch} = 2R_{C,S} + \rho_S L_{Ch}$, where $R_{total} = V_{DS}/I_{DS}$ is the total resistance, R_{Ch} is device channel resistance, $2R_{C,S}$ is the combined contact resistance ($R_{C,S}$) associated with the source and drain electrodes, and ρ_S is the resistivity of an individual *s*-SWNT. Therefore, $2R_{C,S}$ and ρ_S can be extracted from the intercept and slope, respectively, of the linear fit of the R_{total} *versus* L_{Ch} plot.[28] Figure 2e plots linear fits of averaged resistance measured in the ON state ($1/\bar{G}_{ON,S}$) as a function of L_{Ch} under different V_{OV}. $2\bar{R}_{C,S}$, determined from the *y*-intercept of each fitting, is plotted in Figure 2f. The results show that $2\bar{R}_{C,S}$ is ~40 ± 20 kΩ with no significant dependence on V_{OV} within experimental uncertainties. This number is quantitatively similar to values reported in previous studies of both individual nanotube devices (12−32 kΩ)[4,6,9] and array devices (30−50 kΩ)[7,8,35] using CVD-grown *s*-SWNTs

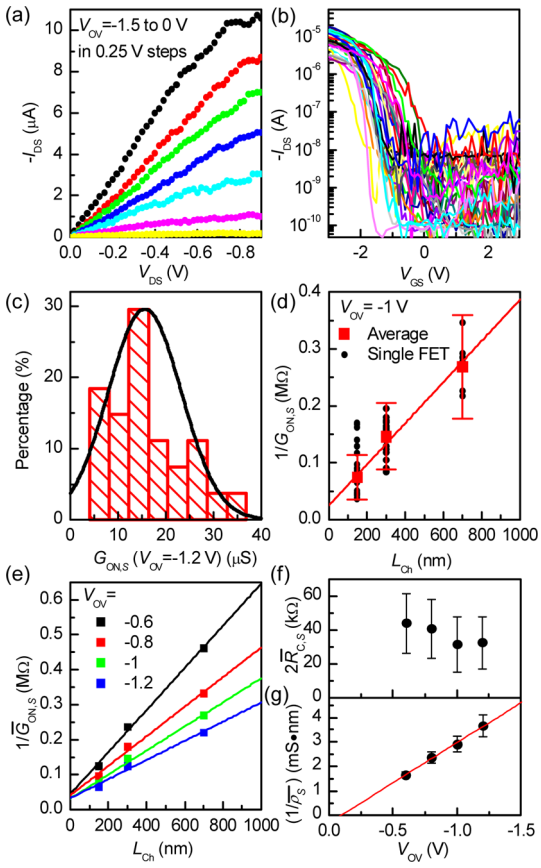

Figure 2. (a) Typical current−voltage characteristics of a FET based on an individual solution-processed *s*-SWNT with L_{Ch} of 150 nm. From top to bottom, V_{OV} varies from −1.5 to 0 V with a step of 0.25 V. (b) Logarithmic scale plot of transfer curves of 30 *s*-SWNT FETs with L_{Ch} of 150 nm. Applied V_{DS} is −0.5 V. (c) Distribution of $G_{ON,S}$ under V_{OV} of −1.2 V for *s*-SWNT FETs with L_{Ch} of 150 nm. The black line is Gaussian fit to the data. (d) Device resistance ($1/G_{ON,S}$) as a function of L_{Ch} under V_{OV} of −1 V. The red squares with error bars represent the average of values from each device (black circles). The red solid line represents a linear fit. (e) Average device resistance of *s*-SWNTs ($1/\bar{G}_{ON,S}$) as a function of L_{Ch} at V_{OV} of −0.6 V (black), −0.8 V (red), −1 V (green), and −1.2 V (blue) from top to bottom. Solid lines represent linear fits. (f) $2\bar{R}_{C,S}$ extracted from the intercepts in frame (e) as a function of V_{OV}. (g) Averaged conductivity of *s*-SWNTs ($1/\bar{\rho}_S$), determined from the reciprocal of slopes of the linear fittings in frame (e), as a function of V_{OV}. Red solid line represents a linear fit.

with similar diameters and metallization. The V_{OV} dependence of averaged ρ_S ($\bar{\rho}_S$) shown in Figure 2g can be utilized to extract $\bar{\mu}_{FE}$ according to

$$\bar{\mu}_{FE} = \frac{L_{Ch}}{C_G}\frac{d(1/\bar{\rho}_S)}{dV_{OV}} \quad (1)$$

The gate capacitance (C_G) is defined as

$$C_G = L_{Ch}\left[C_Q^{-1} + \frac{\ln(2t_{ox}/\bar{r})}{2\pi\varepsilon_0\varepsilon_r}\right]^{-1} \quad (2)$$

where C_Q^{-1} is the quantum capacitance (0.4 nF·m^{-1}),[36] t_{ox} = 10 nm is the dielectric thickness, $\bar{r}$ = 0.7 nm is the average radius of the solution-processed SWNTs, and ε_0 is vacuum permittivity. The relative dielectric constant of the air/SWNT/HfO_2 sandwich structure (ε_r) is

approximated as $\varepsilon_r = (\varepsilon_{air} + \varepsilon_{HfO_2})/2 = (1 + 16)/2 = 8.5$, where $\varepsilon_{air} = 1$ and $\varepsilon_{HfO_2} = 16$ are relative dielectric constant of air and CVD HfO_2, respectively. We find that the linear fit of data shown in Figure 2g gives a $\bar{\mu}_{FE}$ of $\sim$313 $cm^2\,V^{-1}\,s^{-1}$. This value is significantly lower than average values previously reported for CVD-grown nanotubes, which are typically in the range of 2200−10 000 $cm^2\,V^{-1}\,s^{-1}$ extracted *via* TLM from array devices with long L_{Ch}[7,8] and in the range of 1500−3000 $cm^2\,V^{-1}\,s^{-1}$ extracted *via* TLM from individual nanotube devices with similar submicrometer L_{Ch}[9,37] but close to $\bar{\mu}_{eff}$ ($\sim$200 $cm^2\,V^{-1}\,s^{-1}$)[24] of high-quality solution-processed SWNT transistors with long L_{Ch} ($\sim$1 μm). These results suggest that, compared to CVD-grown nanotubes, solution-processed SWNTs possess a higher level of structural defects induced during the purification and suspension processes, which severely limit $\bar{\mu}_{FE}$ due to much stronger defect-induced carrier scattering. However, such defects do not degrade the quality of the electrical contact formed between the nanotube and metal electrodes. On the contrary, they might actually improve the contact by breaking translational symmetry and/or improving metal−SWNT binding to allow easy conduction of electrons from one-dimensional nanotubes to free-electron metals.[38] Therefore, for short-channel nanotube FETs operating in the quasi-ballistic regime, where electron transport is mainly limited by the contacts, solution-processed *s*-SWNTs will provide performance similar to that of CVD tubes. For a hypothetical device using an array of parallel *s*-SWNTs to achieve lower parasitic resistance than that of state-of-the-art planar Si devices, whose typical combined contact resistance is less than 100 $\Omega\cdot\mu$m,[39] the tube density needs to be above 400 tubes/μm.

Since $2\bar{R}_{C,S}$ is only weakly dependent on V_{GS}, we can assume that most of the solution-processed *s*-SWNTs, like their CVD-grown counterparts,[4,7,9] form an Ohmic contact with Pd. Therefore, the invariability of $2R_{C,S}$ against V_{GS} enables us to obtain $2R_{C,S}$ and μ_{FE} of each device based on YFM. Such information could verify results determined based on the averaged collective behavior of nanotube FETs from TLM and provide more insight into device variability. As with the TLM, device resistance can be expressed as

$$R_{total} = 2R_{C,S} + R_{Ch} \quad (3)$$

At small V_{DS}, R_{Ch} of a SWNT FET operating in diffusive transport regime can be phenomenologically approximated as[40]

$$R_{Ch} \approx \frac{L_{Ch}^2}{\mu_{FE}C_G(V_{GS} - V_T)} = \frac{1}{G_m(V_{GS} - V_T)} \quad (4)$$

where $G_m = (\mu_{FE}C_G)/L_{Ch}^2$ is the transconductance parameter. Therefore, eq 3 can be converted to

$$\frac{V_{DS}}{I_{DS}} = \frac{1}{G_m(V_{GS} - V_T)} + 2R_{C,S} \quad (5)$$

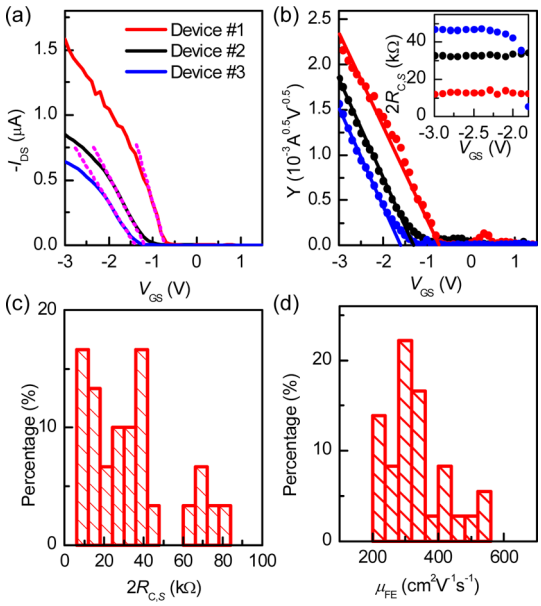

Figure 3. (a) Transfer characteristics of three typical *s*-SWNT FETs, device #1 (red), #2 (black), #3 (blue), from top to bottom, with L_{Ch} of 150 nm. Applied V_{DS} is −50 mV. Magenta dotted lines serve as visual guide to extract g_m and V_{Text} of each device. (b) Calculated Y function and 2 $R_{C,S}$ (inset) for the three devices shown in frame (a) as a function of V_{GS}. Solid lines represent linear fits. Distribution of $2R_{C,S}$ (c) and μ_{FE} (d) extracted from 36 FETs that use solution-processed *s*-SWNTs with L_{Ch} of 150 nm.

I_{DS} can now be written as

$$I_{DS} = \frac{V_{DS}G_m(V_{GS} - V_T)}{1 + 2R_{C,S}G_m(V_{GS} - V_T)} \quad (6)$$

Assuming a constant $2R_{C,S}$, the device transconductance, g_m, can be obtained from eq 6 as

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \frac{1}{[1 + 2R_{C,S}G_m(V_{GS} - V_T)]^2} \quad (7)$$

The Y function is defined as[29]

$$Y = \frac{I_{DS}}{\sqrt{g_m}}\sqrt{V_{DS}G_m}(V_{GS} - V_T) \quad (8)$$

where we can see that the Y function is independent of $R_{C,S}$, and μ_{FE} can be extracted from the slope of the Y *versus* V_{GS} plot with intrinsic V_T obtained from the *x*-axis intercept. With known μ_{FE} and V_T, $2R_{C,S}$ of a specific device can be acquired according to

$$2R_{C,S} = \frac{V_{GS}}{I_{DS}} - \frac{1}{G_m(V_{GS} - V_T)} \quad (9)$$

Transfer curves of three typical *s*-SWNT FETs, measured with V_{DS} of −50 mV and V_{GS} swept between ±3 V, are shown in Figure 3a. These three FETs demonstrate very different g_m, with the g_m of device #1 about two times higher than that of device #3. However, the plots of Y function of these devices (Figure 3b) reveal that they have almost identical μ_{FE}, as evident from their similar slopes. In addition, by comparing panels a and b of Figure 3, we find that the deviation of extrapolated

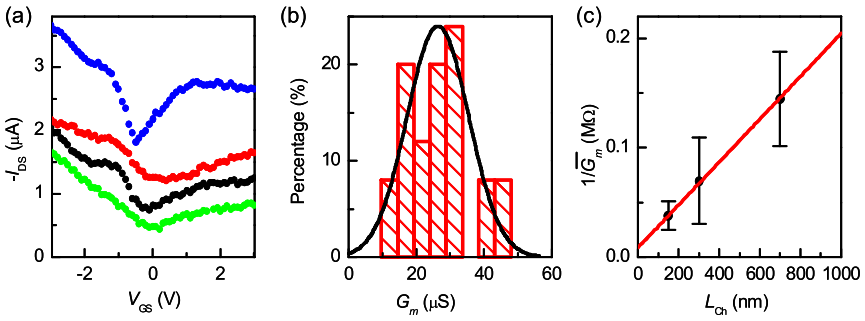

Figure 4. (a) Transfer characteristics of several *m*-SWNTs exhibiting a small bang gap. Applied V_{DS} is −50 mV. (b) G_m distribution of 25 *m*-SWNTs with L_{Ch} of 150 nm, measured with gate electrode grounded. The black solid line is Gaussian fit to the data. (c) Average resistance of *m*-SWNTs ($1/\bar{G}_m$) as a function of L_{Ch}. Red solid line represents a linear fit.

V_{Text} from extracted intrinsic V_T increases from ~0 V for device #1 to ~0.15 V for device #2 and ~0.3 V for device #3, indicating the increase of device parasitic resistance. The inset of Figure 3b presents the calculated $2R_{C,S}$ of each device as a function of V_{GS} according to eq 9. Devices #2 and #3 indeed have much higher $2R_{C,S}$ than that of device #1, explaining their lower g_m observed in Figure 3a. We analyze 36 devices and plot the distribution of extracted $2R_{C,S}$ and μ_{FE} in Figure 3c, d, with their means and standard deviations calculated to be 300 ± 100 $cm^2\ V^{-1}\ s^{-1}$ and 30 ± 20 kΩ, respectively. These values are quantitatively comparable to $2\bar{R}_{C,S}$ and $\bar{\mu}_{FE}$ obtained by TLM. The variation of $2R_{C,S}$ suggests the device performance fluctuation expected for ultimately scaled nanotube FETs, where effects from charge trapping or μ_{FE} variation caused by defects are largely eliminated. The presence of a group of *s*-SWNTs with high $2R_{C,S}$ (above 60 kΩ) could be caused by nanotube diameter distribution. The barrier for hole transport through a nanotube−metal contact (Φ_p) can be described as

$$\Phi_p = \left(\Phi_{SWNT} + \frac{0.39\ eV}{r\ (nm)}\right) - \Phi_m \qquad (10)$$

where *r* is nanotube radius and Φ_{SWNT} and Φ_m are work function of *s*-SWNT and metal contact, respectively.[41] As shown in Figure 1d, there are a fraction of nanotubes with *r* less than 0.5 nm. For those nanotubes, a positive Schottky barrier is formed for hole transport with Pd contacts, leading to high $2R_{C,S}$. Further tightening up the diameter distribution of solution-processed SWNTs by techniques like iterative density gradient ultracentrifugation[16] will help minimize device variation for SWNT FETs operating in the quasi-ballistic regime.

Another important aspect to investigate is the scaling behavior of *m*-SWNTs. The conductance of some *m*-SWNTs can be weakly modulated by V_{GS}, due to the presence of Mott insulating state or symmetry-breaking defects, strains, and twists,[42,43] as shown in Figure 4a. Here we define the conductance of *m*-SWNTs (G_m) as the device conductance measured with the gate electrode grounded. G_m, same as $G_{ON,S}$, has a wide distribution as plotted in Figure 4b, with its average ($\bar{G}_m$, 30 ± 10 μS) about 2−3 times higher than $\bar{G}_{ON,S}$ (15 ± 8 μS under $V_{OV} = -1.2$ V). Figure 4c presents the dependence of $1/\bar{G}_m$ on L_{Ch}. The extracted average resistivity of *m*-SWNTs ($\bar{\rho}_m$) is 200 ± 10 kΩ/μm, which is much higher than that of typical CVD-grown nanotubes extracted from both array (24−80 kΩ/μm)[7,8] and individual nanotube devices (6−30 kΩ/μm),[9,44,45] while the extracted average overall contact resistance ($2\bar{R}_{C,m}$) is 9 ± 2 kΩ, comparable to values from previous reports on CVD-grown nanotubes (6−20 kΩ).[7,9,37,44,46] These observations suggest that the behaviors of solution-processed *m*-SWNTs are similar to their semiconducting counterparts, where a higher level of structural defects hinders their electron transport with increased scattering but does not degrade the contacts between nanotubes and metal electrodes. Compared to *s*-SWNTs, these *m*-SWNTs demonstrate a comparable channel quality, as evident from their similar resistivity ($\bar{\rho}_m$, 200 ± 10 kΩ/μm, *vs* $\bar{\rho}_S$ at $V_{OV} = -1.2$ V, 270 ± 30 kΩ/μm), but with a much lower contact resistance ($2\bar{R}_{C,m}$, 9 ± 2 kΩ, *vs* $2\bar{R}_{C,S}$, 40 ± 20 kΩ), which leads to higher conductance, especially for short-channel devices. These results suggest that, for an ultimately scaled FET fabricated on an array of parallel nanotubes, a *m*-SWNT existing in the channel can carry 3−5 times more current than a semiconducting one. Thus, the presence of *m*-SWNTs will more severely reduce device ON/OFF ratio for devices with shorter L_{Ch}.

CONCLUSION

In conclusion, a systematic study of contact resistance, μ_{FE}, and conductivity of solution-processed SWNTs based on both TLM and YFM indicates that defects in those nanotubes, which might result from purification and/or suspension processes and act as localized electron scattering centers, limit their electron transport capability. However, those structural defects do not affect the quality of the electrical contacts between nanotube and metal electrodes, as evident from the fact that their extracted contact resistance is comparable to that of CVD-grown nanotubes

from previous reports. Therefore, solution-processed *s*-SWNTs are expected to provide performance similar to that of CVD-grown nanotubes in ultimately scaled FETs, where electron transport is largely limited by contacts rather than channel scattering. Most *s*-SWNTs are expected to form Ohmic contacts with Pd; however, a considerable distribution of $2R_{C,S}$ extracted from individual nanotube transistors is observed, which is partially caused by the formation of Schottky barriers between small-diameter nanotubes and metal electrodes. This variation of $2R_{C,S}$ indicates the performance fluctuation of ultimately scaled SWNT FETs, which could be reduced by tightening the nanotube diameter distribution. Solution-processed *m*-SWNTs, on average, form a less resistive contact with metal compared to *s*-SWNTs. Therefore, the presence of *m*-SWNTs in the channel will show a greater impact on device ON/OFF ratio for FETs with more scaled L_{Ch}. These results are not only important for understanding the materials science and device physics of solution-processed SWNTs but also useful for future materials development and device optimization for high-performance nanotube-based electronics aiming at extending the limit of CMOS scaling.

METHODS

Processing of Nanotubes. Three milligrams of SWNTs synthesized by arc-discharge method and purified by both heat and acid treatments (Hanwha Nanotech, ASP-100F) and 3 mg of poly(*m*-phenylenevinylene-*co*-2,5-dioctoxy-*p*-phenylenevinylene) (PmPV) were added into 15 mL of DCE.[47] The mixture was sonicated for 60 min with a high-power horn sonicator (600 W, 95% amplitude, 20 kHz) and then centrifuged at 35 000 rpm for 2 h (Beckman Coulter, Optima L-100 XP ultracentrifuge). After centrifugation, the supernatant was collected and filtered through a Teflon filter paper (Fluopore, 0.22 μm pore) and then resuspended in DCE by brief bath sonication. The filtration and resuspension were repeated for four cycles to remove extra PmPV surfactant.[48] The SWNT suspension was centrifuged again at 35 000 rpm for 2 h. The supernatant was collected, diluted, and sonicated again with the high-power horn sonicator for 10 min before use. The p++ Si substrate with 10 nm HfO_2 was soaked in SWNT DCE suspension for 2 min, washed by isopropyl alcohol, and blown dry with nitrogen. The as-deposited SWNTs were further annealed under vacuum with a base pressure less than 10^{-6} Torr at 400 °C for 2 min. EBL was performed to pattern electrodes.

Characterizations of Nanotubes. Optical image of device arrays was taken by a Nikon eclipse L200 microscope. SEM images of devices were acquired using Zeiss/LEO 1560. Raman spectrum was measured using LabRAM ARAMIS micro-Raman instrument with an excitation wavelength of 532 nm. AFM images of nanotubes were taken with a Dimension 3000 instrument in tapping mode. Electrical properties of SWNT devices were measured by a semi-automated probe station in air and at room temperature.

Conflict of Interest: The authors declare no competing financial interest.

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